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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/681,643	05/15/2001	Takatoshi Tsujimura	JP920000112US1	8744

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THE LAW OFFICE OF IDO TUCHMAN
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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/681,643	TSUJIMURA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 15, 2005 have been fully considered but they are not persuasive.

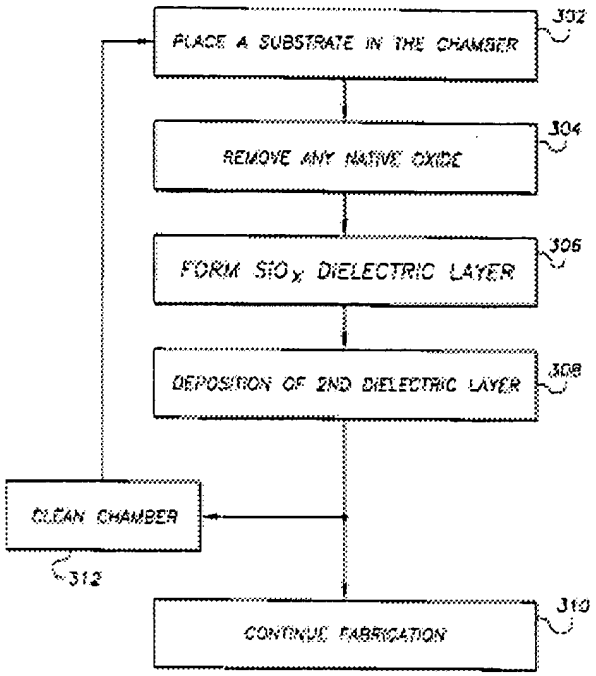
2. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

3. Applicant contends that because the primary reference fails to disclose forming an oxide on the inner wall of a chamber, the primary reference is not obvious to Applicants claimed invention. Ohnuma et al., U.S. Patent 6,072,193 herein known as Ohnuma substantially teaches Applicants claimed limitations and although Ohnuma is silent with respect to an oxide being formed on the inner wall of a chamber before applying a dopant to form a source and drain, it would have been obvious to combine Gardner et al., U.S. Patent 6,066,519 herein known as Gardner to disclose that oxides are formed on the chamber wall. Because Ohnuma teaches forming a top gate TFT, it is obvious that a gate oxide is formed prior to the source and drain being formed since Ohnuma teaches forming an oxide film on the glass substrate prior to forming an amorphous silicon film, which is doped after forming the insulating film. The combined teachings would suggest that because the oxide film is formed prior to the gate electrode and prior to the formation of the source and drain regions, no doping has taken place during oxide formation and only afterwards. Gardner suggest that when forming oxides in a

vacuum chamber, oxide film is also formed on the inner chamber wall, therefore Applicants arguments are moot.

4. Applicant contends that neither Ohnuma nor Gardner could possibly form an oxide on the chamber wall because the combined art only suggest removing residual oxide from the chamber wall.

5. In response to Applicants contention that the combined teachings fail to disclose forming an oxide on the chamber wall, please note the following. Gardner discloses a diagram providing the steps of after forming the SiO_x dielectric layer (step 306) and the second dielectric layer (step 308), the chamber cleaning step can be incorporated in the fabrication steps. This would suggest that cleaning the chamber takes place after the formation of forming the dielectric layers. Since cleaning normally is defined as removing something unwanted, the dielectric layer is removed from the chamber and the chamber comprises chamber walls. Please see the diagram below which discloses the process steps of Gardner.



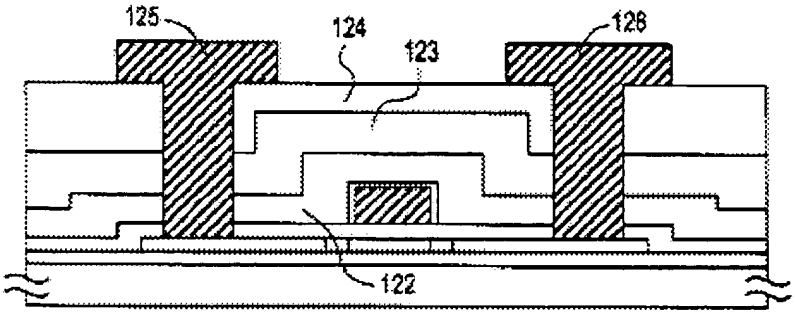
Claim Rejections - 35 USC § 103

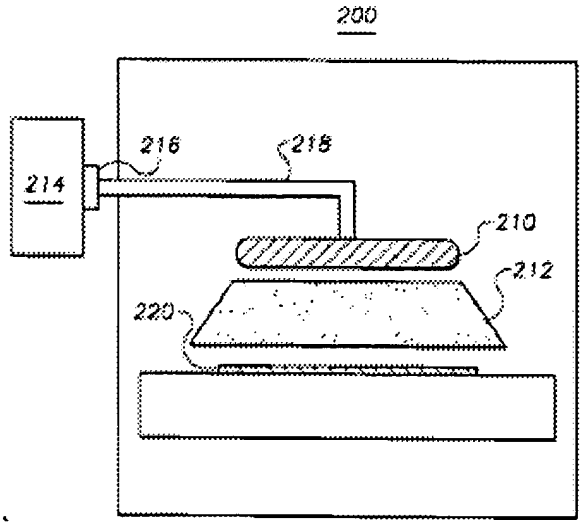
6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnuma et al., U.S. Patent 6,072,193 in view of Gardner et al., U.S. Patent 6,066,519.

FIG.6A





8. Pertaining to claims 1 and 2, Ohnuma discloses a semiconductor process substantially as claimed. See **FIGS. 1A-2D**, where Ohnuma teaches a manufacturing method of an active matrix device (column 17, line 62) including a top gate type TFT, which comprises a process of forming the top gate type TFT, wherein the process of forming the top gate type TFT includes the steps of:

arranging a substrate **101** having source **125** and drain electrodes **126** formed therein in

the processing chamber; doping the source and drain electrodes with P (phosphorous), (column 3, lines 51-54); and forming an a-Si layer **103** and a gate insulating film **104** in the processing chamber; and

wherein forming the oxide film on the inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P. However, Ohnuma fails to disclose forming an oxide film on an inner wall of a CVD processing chamber. Gardner teaches forming an oxide on an inner wall of a CVD processing chamber (column 6, lines 8-14). In view of Gardner, it would have been obvious to one of ordinary skill in the art because when forming a gate dielectric residual oxide forms on the chamber walls (column 6, lines 10-12).

9. Pertaining to claim 2, Ohnuma fails to disclose removing the oxide film form the inner wall after the step of forming the a-Si layer and the gate insulating layer. Gardner teaches the step of removing oxide between runs. In view Gardner, it would have been obvious to one of ordinary skill in the are to remove oxide from the chamber walls after the step of forming the a-Si layer and the gate insulating film because the a silicon gate dielectric layer may be formed in a highly controlled manner (column 6, lines 21-23).

10. Pertaining to claim 3, Ohnuma teaches a manufacturing method of an active matrix device according to claim 1,

wherein the oxide film contains SiOx.

11. Pertaining to claim 4, Ohnuma teaches a manufacturing method of an active matrix device according to claim 1, wherein the active matrix device is a liquid crystal display (column 17, line 62).

12. Pertaining to claim 5, Ohnuma teaches a manufacturing method of an active matrix device according to claim 1, wherein the active matrix device is an electroluminescence display (column 17, line 62).

13. Pertaining to claim 6, Ohnuma teaches a manufacturing method of an active matrix device according to claim 2, wherein the oxide film contains SiO_x.

14. Pertaining to claim 7, Ohnuma teaches a manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is a liquid crystal display.

15. Pertaining to claim 8, Ohnuma teaches a manufacturing method of an active matrix device according to claim 3, wherein the active matrix device is a liquid crystal display.

16. Pertaining to claim 9, Ohnuma teaches a manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is an electroluminescence display.

17. Pertaining to claim 10, Ohnuma teaches a manufacturing method of an active matrix device according to claim 3, wherein the active matrix device is an electroluminescence display.

18. Pertaining to claim 17, Ohnuma in view of Gardner teaches a manufacturing method of an active matrix device according to claim 1, further comprising heating the inner wall of the CVD processing chamber. Gardner discloses outgassing the oxide and controlling the temperature of the of the chamber (column 3, lines 22-40).

19. Pertaining to claim 18, Ohnuma teaches a manufacturing method of an active matrix device according to claim 1, wherein the oxide film is selected from the group of SiO_x

20. Pertaining to claim 19, Ohnuma teaches a manufacturing method of an active matrix device including a top gate TFT, which comprises a process of forming the top gate TFT, wherein the process of forming the top gate TFT includes the steps of:

forming an oxide film on **102/109** on a substrate **101** (please note that the Examiner takes the position that oxide film formation is well known to incorporate in forming a TFT);

arranging a substrate **101** having source and drain electrodes formed therein in the processing chamber;

doping the source and drain electrodes with P;

forming an a-Si layer and a gate insulating film in the processing chamber; and

the gate oxide is formed before doping the source and drain electrodes with P (phosphorus). However, Ohnuma fails to disclose that during the formation of the oxide layer on the substrate, oxide formation occurs on the CVD processing chamber with a film of any thickness including at least 50 nm in thickness. Gardner teaches forming an oxide on an inner wall of a CVD processing chamber (column 6, lines 8-14). In view of Gardner, it would have been obvious to one of ordinary skill in the art because when forming a gate dielectric residual oxide forms on the chamber walls (column 6, lines 10-12).

21. Pertaining to claim 20, the combined teachings discloses a manufacturing method of an active matrix device according to claim 19, wherein the oxide is approximately 100 nm (column 7, lines 9-10).

22. Pertaining to claim 21, Ohnuma in view of Gardner discloses a manufacturing method of an active matrix device according to claim 19, wherein forming the oxide film on the inner wall of the CVD chamber is performed before doping the source and drain electrodes with P (please see the rejection as applied to claim 1 above).

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC